



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,813	09/17/2003	Junichi Nakamura	117212	4050
25944	7590	12/23/2005		EXAMINER
OLIFF & BERRIDGE, PLC				PIZIALI, JEFFREY J
P.O. BOX 19928				
ALEXANDRIA, VA 22320			ART UNIT	PAPER NUMBER
			2673	

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,813	NAKAMURA, JUNICHI	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 28 September 2005.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1,4-12,14 and 15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1,4-12,14 and 15 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 17 September 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>4 November 2005</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____ .

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 4-10, 12, 14, and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Murata et al (US 6,876,348 B2).

Regarding claim 1, Murata discloses an optoelectronic-device substrate, comprising: a pixel electrode [Figs. 3 and 4; 100]; a storage unit [Figs. 3 and 4; 200] for storing pixel data (see Column 3, Lines 23-36); a phase-inversion circuit [Fig. 4; 15, 16] that outputs a phase-inversion signal [Fig. 4; SW-A control signal] for converting a phase of pixel data from the storage unit (see Column 4, Lines 1-50); a first switch [Fig. 4; SW-A] for generating a data-inversion signal [Fig. 5; "Pixel" signal], based on the phase-inversion signal; and a second switch [Fig. 4; SW-B] for switching between the data-inversion signal [Fig. 5; 5-to-10 volts] from the first switch and a zero-data signal [Fig. 5; 5.5-to-9 volts], the second switch selecting the data-inversion signal

when pixel data is stored in the storage unit [Fig. 5; SRAM driving mode], and the zero-data signal when the pixel data is not stored in the storage unit [Fig. 5; normal/writing mode], the selected one of the data-inversion signal and the zero-data signal being transmitted to the pixel electrode (see Column 4, Line 51 - Column 6, Line 52 -- in particular, Column 4, Line 64 - Column 5, Line 12).

Regarding claim 4, Murata discloses the storage unit being formed as an SRAM (see Column 3, Lines 60-67).

Regarding claim 5, Murata discloses the memory-cell array including: a plurality of first signal lines [Fig. 3; 17] to connect one group of address terminals included in one group of the storage units in parallel, the one group of the storage units being provided along a row direction; a plurality of second signal lines [Fig. 3; 11] to connect one group of data terminals included in one group of the storage units in parallel, the one group of the storage units being provided along a column direction; and a plurality of third signal lines [Fig. 3; 18] to connect one group of phase-inversion terminals included in one group of the storage units in parallel, the one group of the storage units being provided along the row direction or the column direction; and the optoelectronic-device substrate further including: a first driver circuit [inherent but not illustrated] to transmit address signals in sequence to the storage units via the plurality of first signal lines, the storage units being provided along the row direction; a second driver circuit [Fig. 3; 19] to transmit the pixel data to the storage units at one time via the plurality of second signal lines, the storage units being provided along the column direction; and a third driver

circuit [inherent but not illustrated] to transmit phase-inversion signals to each group of the storage units via the plurality of third signal lines, the group of the storage units being provided along the row direction or the column direction (see Column 3, Lines 23-59).

Regarding claim 6, Murata discloses the third driver circuit having a phase-inversion circuit [Fig. 4; 15, 16] to invert the phase of the pixel data, and the phase-inversion circuit inverting the phase of the pixel data before the pixel data is transmitted to the storage units (see Fig. 5; Column 4, Line 51 - Column 5, Line 30).

Regarding claim 7, Murata discloses the memory-cell array including: a plurality of first signal lines [Fig. 3; 17] to connect one group of address terminals included in one group of the storage units in parallel, the one group of the storage units being provided along a row direction; a plurality of second signal lines [Fig. 3; 11] to connect one group of data terminals included in one group of the storage units in parallel, the one group of the storage units being provided along a column direction; and a plurality of third signal lines [Fig. 3; 18] to connect one group of phase-inversion terminals included in one group of the storage units in parallel, the one group of the storage units being provided along the row direction or the column direction; and wherein the optoelectronic-device substrate further including: a row-address-decoder driver circuit [inherent but not illustrated] to transmit row-address data for selecting any of rows of the storage units via the plurality of first signal lines, the storage units being provided along the row direction; a column-address-decoder driver circuit [Fig. 3; 19] to transmit column-address data to select any of columns of the storage units via the plurality of second signal lines, the storage units being

provided along the column direction, and the pixel data output to the storage units designated by the row-address data and the column-address data; and a phase-inversion driver circuit [inherent but not illustrated] to transmit a phase-inversion signal to each group of the storage units via the plurality of third signal lines, the each group of the storage units being provided along the row direction or the column direction (see Column 3, Lines 23-59).

Regarding claim 8, Murata discloses the phase-inversion driver circuit having a phase-inversion circuit [Fig. 4; 15, 16] to invert the phase of the pixel data, the phase-inversion circuit inverting the phase of the pixel data in a predetermined cycle regardless of the number of the storage units whose display information is rewritten according to the pixel data (see Fig. 5; Column 4, Line 51 - Column 5, Line 30).

Regarding claim 9, Murata discloses a digitally-driven liquid-crystal display, comprising the optoelectronic-device substrate; a counter substrate [Fig. 4; 12]; a liquid crystal layer [Fig. 4; 14] provided between the optoelectronic device substrate and the counter substrate; and a common electrode [Fig. 4; 13] to supply a voltage having a potential [Fig. 5; 5-to-10 volts] that is equivalent to the potential of zero data transmitted to the optoelectronic-device substrate (see Fig. 5; Column 4, Line 51 - Column 5, Line 30).

Regarding claim 10, Murata discloses an electronic apparatus, comprising the digitally driven liquid crystal display; and a display unit to display an image through the digitally-driven liquid-crystal display (see Column 3, Lines 15-20).

Regarding claim 12, this claim is rejected by the reasoning applied in rejecting claim 1; furthermore, Murata discloses a method of driving an optoelectronic-device substrate that includes a memory-cell array [Fig. 3; 200] including a plurality of storage units that is arranged in matrix form along a row direction and a column direction and that is digitally driven, and a pixel electrode [Fig. 3; 100] to retrieve pixel data stored in the storage units as an electrical signal, the method comprising: performing at least one of inverting the phase of the pixel data before the pixel data is transmitted to the storage units, and inverting the phase of the pixel data after the pixel data is transmitted to the storage units (see Column 4, Line 64 - Column 5, Line 12).

Regarding claim 14, Murata discloses the performing including selecting the storage units provided along the row direction in sequence, and inverting the phase of the pixel data at the same time (see Fig. 5; Column 4, Line 64 - Column 5, Line 12).

Regarding claim 15, Murata discloses the performing including transmitting a cycle with which the phase-inversion signal to the storage units provided along the row direction, and making a cycle with which the pixel data is transmitted to the storage units provided along the row direction variable so that the cycles can change [see Fig. 5] in synchronization, whereby a cycle of sub-frames is made variable so as to present gray scale [i.e. tone levels, white, black, brightest white, and darkest black] (see Column 4, Line 64 - Column 5, Line 30).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murata et al (US 6,876,348 B2).

Regarding claim 11, Murata discloses a control circuit to control the digitally-driven liquid-crystal display (see Column 3, Lines 23-36); but does not expressly disclose a projector. However, it was well known and commonly understood at the time of invention to use a digitally-driven liquid-crystal display as projector, comprising: a light-source unit to supply projection light; and a projection-lens system to magnify and project an image of the digitally-driven liquid-crystal display. Therefore, it would have been obvious at the time of invention to one skilled in the art to use Murata's optoelectronic substrate within such a projector, so as to provide an imaging device for a large audience, while keeping display manufacturing costs and power consumption low.

Response to Arguments

6. Applicant's arguments filed 28 September 2005 have been fully considered but they are not persuasive. The applicant contends "the normal/writing mode in Fig. 5 of [the cited prior art of Murata et al (US 6,876,348 B2)] uses an analog potential, not a zero-data signal" (see Page 9, Lines 18-19 of the Amendment submitted 28 September 2005). The applicant continues that

Murata's "analog potential cannot be zero because, if the analog potential were zero, there would be no potential difference between the pixel electrode and the counter electrode" (see Page 9, Lines 22-24 of the Amendment submitted 28 September 2005). However, the examiner respectfully disagrees. Although Murata's Fig. 5 illustrates "the video data in [one] embodiment is analog multi-tone data varying between 9V and 5.5V" (see Column 5, Lines 15-16), Murata explicitly teaches in yet another embodiment that "the high power supply voltage is 5V, and the low power voltage is 0V" (see Column 9, Lines 38-40). Certainly, one skilled in the art would consider Murata's zero voltage level as constituting "a zero-data signal" as presently claimed. Moreover, it remains the examiner's respectful position that due to the sheer breadth of claim language (particularly pertaining to "a zero-data signal"), one skilled in the art would consider any voltage level (9V or 5.5V, for example) that sets Murata's pixels to black (or to white -- depending on whether the display is ordinarily black or whether the display is ordinarily white) as constituting "a zero-data signal." By such reasoning, rejection of the claims is deemed proper, necessary, and thereby maintained at this time.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

Art Unit: 2673

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



J.P.
15 December 2005



BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600